

Introduction To RTL Synthesis

Introduction

In the tutorial 4 (Simple RTL project) we have created a new RTL project using Vivado and we have validated its behavior in simulation using the Vivado Simulator (XSIM) in the tutorial 5 (Behavioral Simulation with the Vivado Simulator). In this tutorial we will run the synthesis on this project to understand this process.

What is synthesis?

According to the Xilinx Glossary (<http://www.xilinx.com/company/terms.htm#S>), synthesis is “a process that starts from a high level of logic abstraction (typically Verilog or VHDL) and automatically creates a lower level of logic abstraction using a library containing primitives”. To be simpler, the synthesis is a process that try to realize the behavior described in the sources files (Verilog, VHDL...) using FPGA element. It converts your RTL code into FPGA elements.

Synthesize the design

Open the project and synthesize the design clicking on “Run Synthesis” in the “Flow Navigator”.

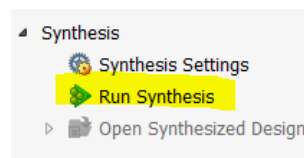


Figure 1 - Run Synthesis

When the Synthesis is done a “Synthesis Completed” window should appears. Select “Open Synthesized Design” and click “OK”.

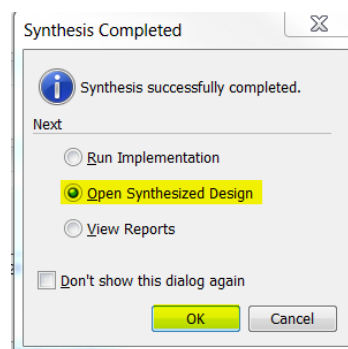


Figure 2 - Synthesis Completed window

In the “Flow Navigator”, click on “Schematic” under “Synthesized Design” to open the synthesized design schematic.

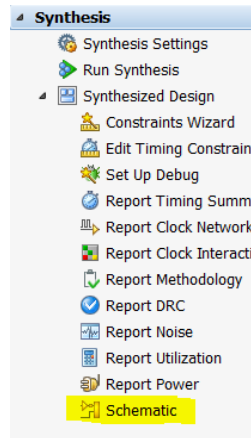


Figure 3 - open the synthesized design schematic

We can now see the synthesized design schematic. In this tutorial, we won't talk about the IBUF and OBUF elements.

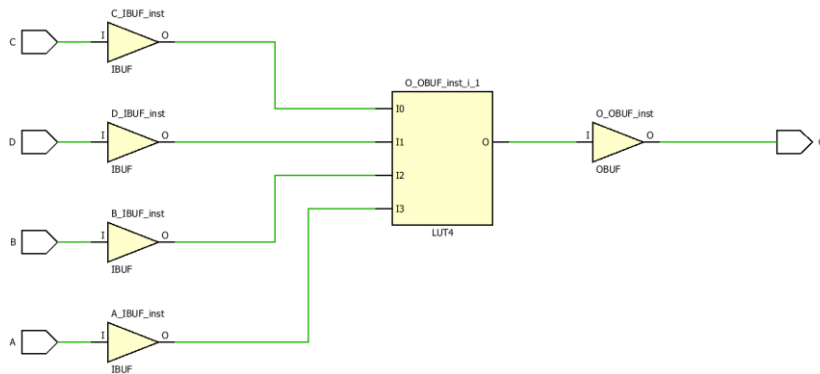


Figure 4 - synthesized design schematic

On this schematic, we can see that our AND and OR gates has been replaced by a LUT4 (Look Up Table). This is because the FPGA does not have these simple gates, so LUTs, which are basic FPGA elements, will be used to replace it. If we select the LUT4 in the schematic, we can see its "Truth Table" in the "Cell Properties" window.

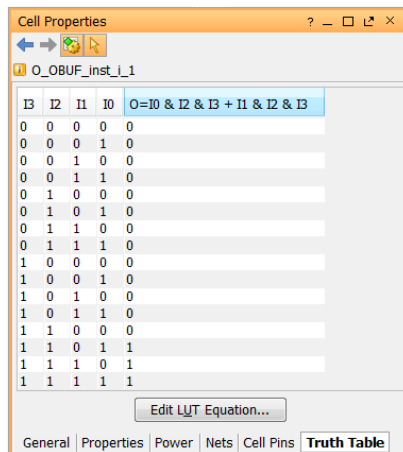


Figure 5 – LUT Truth Table

In this “*Truth Table*” we can see that the Output O is high in 3 cases. As the A, B, C and D inputs are connected respectively to the ports I3, I2, I0 and I1 of the LUT, the output is high:

- When A, B and C are high and D is low
- When A, B and D are high and C is low
- When A, B, C and D are high

This is what we expect.

In the “*Cell Properties*” we also can see the equation of the truth table:

- $O = I0 \& I2 \& I3 + I1 \& I2 \& I3$
- So $O = C \& B \& A + D \& B \& A$ with our port names which is a development of our initial equation $((A \& B) \& (C + D))$